

JUL 15 2003

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Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Date Submitted: 7/15/03

(use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

Application Number	09/927,648
Filing Date	08/13/2001
First Named Inventor	Thomas H. Lee
Group Art Unit	2818
Examiner Name	Howard Weiss
Attorney Docket Number	035905-0104

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
[Signature]	C9	5,999,453		Kawata	12/7/99	
	C10	5,739,567		Wong	4/14/98	
	C11	4,774,556		Fujii et al	9/27/88	
	C12	6,191,459	B1	Hofmann, et al	2/20/01	
	C13	6,157,061		Kawata	12/5/00	
	C14	5,751,012		Wolstenholme, et al	5/12/98	
	C15	5,006,909		Kosa	4/9/91	
	C16	4,967,247		Kaga, et al	10/30/90	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
[Signature]	C17		WO 00/30118		Johnson, et al	5/25/00		Y

NON PATENT LITERATURE DOCUMENTS

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: <u>November 27, 2001</u> (use as many sheets as necessary)				Applicant Number	09/927,648
				Filing Date	08/13/2001
				First Named Inventor	Thomas H. Lee et al.
				Group Art Unit	2818
Examiner Name				Unassigned	
Sheet	1	of	7	Attorney Docket Number	035905/0104

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		Number	Kind Code ² (if known)			
	A51	5,427,979		Chang	6/27/1995	
	A52	5,070,384		McCollum et al.	12/3/1991	
	A53	4,498,226		Inoue et al.	2/12/1985	
	A54	4,489,478		Sakurai	12/25/1984	
	A55	4,272,880		Pashley	6/16/1981	
	A56	5,745,407		Levy et al.	4/28/1998	
	A57	5,535,156		Levy et al.	7/9/1996	
	A58	4,499,557		Holmberg et al.	2/12/1985	
	A59	4,442,507		Roesner	4/10/1984	
	A60	4,507,757		McElroy	3/26/1985	
	A61	4,543,594		Mohsen et al.	9/24/1985	
	A62	4,569,121		Lim et al.	2/11/1986	
	A63	4,646,266		Ovshinsky et al.	2/24/1987	
	A64	4,820,657		Hughes et al.	4/11/1989	
	A65	4,823,161		Mohsen et al.	4/18/1989	
	A66	4,811,114		Yamamoto et al.	3/7/1989	
	A67	4,899,205		Hamdy et al.	2/6/1990	
	A68	3,863,231		Taylor	1/28/1975	
	A69	3,990,098		Mastrangelo	11/2/1976	
	A70	4,146,902		Tanimoto et al.	3/27/1979	
	A71	4,203,123		Shanks	5/13/1980	
	A72	4,203,158		Frohm-Bentchkowsky et al.	5/13/1980	
	A73	4,281,397		Neal et al.	7/28/1981	
	A74	4,419,741		Stewart et al.	12/6/1983	
	A75	4,420,766		Kasten	12/13/1983	
	A76	4,494,135		Moussie	1/15/1985	
	A77	4,922,319		Fukushima	5/1/1990	
	A78	4,943,538		Mohsen et al.	7/24/1990	
	A79	5,070,383		Sinar et al.	5,070,383	
	A80	5,311,039		Kimura et al.	5,311,039	
	A81	5,334,830		Abadeer et al.	5,334,830	
	A82	5,391,907		Jang	2/21/1995	
	A83	5,441,907		Sung et al.	5,441,907	
	A84	5,463,244		De Araujo et al.	5,463,244	
	A85	5,536,968		Crafts et al.	7/16/1996	
	A86	5,675,547		Koga	10/7/1997	
	A87	5,737,259		Chang	4/7/1998	
	A88	5,751,012		Wolstenholme et al.	5/12/1998	
	A89	5,776,810		Guterman et al.	7/7/1998	
	A90	5,835,396		Zhang	11/10/1998	
	A91	5,883,409		Guterman et al.	3/16/1999	
	A92	3,629,863		Neale	12/21/1971	
	A93	3,571,809		Nelson	3/23/1971	

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Sheet	2	of	7

U.S. PATENT DOCUMENTS					
	U.S. Patent Document				
A94	3,573,757		Adams	4/8/1971	
A95	3,699,543		Neale	10/17/1972	
A96	3,846,767		Cohen	11/5/1974	
A97	3,877,049		Buckley	4/8/1975	
A98	3,886,577		Buckley	5/27/1975	
A99	3,922,648		Buckley	11/25/1975	
A100	3,980,505		Buckley	9/14/1976	
A101	4,177,475		Holmberg	12/4/1979	
A102	4,677,742		Johnson	7/7/1987	
A103	3,582,908		Koo	6/1/1971	
A104	3,717,852		Abbas et al.	2/20/1973	
A105	3,787,822		Rigault	1/22/1974	
A106	3,634,929		Yoshida et al.	1/18/1972	
A107	4,881,114		Mohsen et al.	11/14/1989	
A108	5,391,518		Bhushan	2/21/1995	
A109	5,675,547		Koga	10/7/1997	
A110	3,728,695		Frohman-Bentchkowsky	4/17/1973	
A111	4,876,220		Mohsen et al.	10/24/1989	
A112	3,671,948		Cassen et al.	6/20/1972	
A113	3,576,549		Hess	4/27/1971	
A114	5,978,258		Manning	11/2/1999	

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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	09/927,848
Date Submitted: <u>November 27, 2001</u>		Filing Date	08/13/2001
(use as many sheets as necessary)		First Named Inventor	Thomas H. Lee et al.
		Group Art Unit	2818
		Examiner Name	Unassigned
		Attorney Docket Number	035905/0104
Sheet	3 of 7		

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [§]
	A115	JOHN H. DOUGLAS: "The Route to 3-D Chips," High Technology, September 1983, pgs. 55-59, Vol. 3, No. 9, High Technology Publishing Corporation, Boston, MA	
	A116	M. ARIENZO et al.: "Diffusion of Arsenic in Bilayer Polycrystalline Silicon Films," J. Appl. Phys., January 1984, pgs. 365-369, Vol. 55, No. 2, American Institute of Physics	
	A117	O. BELLEZZA et al.: "A New Self-Aligned Field Oxide Cell for Multimegabit Eeproms," IEDM, pgs. 579-582, IEEE	
	A118	S.D. BROTHERTON et al.: "Excimer-Laser-Annealed Poly-Si Thin-Film Transistors," IEEE Transactions on Electron Devices, February 1993, pgs. 407-413, Vol. 40, No. 2, IEEE	
	A119	P. CANDELIER et al.: "Simplified 0.35-µm Flash EEPROM Process Using High-Temperature Oxide (HTO) Deposited by LPCVD as Interpoly Dielectrics and Peripheral Transistors Gate Oxide," IEEE Electron Device Letters, July 1997, pgs. 306-308, Vol. 18, No. 7, IEEE	
	A120	MIN CAO et al.: "A High-Performance Polysilicon Thin-Film Transistor Using XeCl Excimer Laser Crystallization of Pre-Patterned Amorphous Si Films," IEEE Transactions on Electron Devices, April 1996, pgs. 561-567, Vol. 43, No. 4, IEEE	
	A121	MINO CAO et al.: "A Simple EEPROM Cell Using Twin Polysilicon Thin Film Transistors," IEEE Electron Device Letters, August 1994, pgs. 304-306, Vol. 15, No. 8, IEEE	
	A122	BOMY CHEN et al.: "Yield Improvement for a 3.5-ns BICMOS Technology in a 200-mm Manufacturing Line," IBM Technology Products, 1993, pgs.301-305, VLSITSA	
	A123	VICTOR W.C. CHAN et al.: "Three Dimensional CMOS Integrated Circuits on Large Grain Polysilicon Films," IEDM, 2000, IEEE	
	A124	BOAZ EITAN et al.: "Alternate Metal Virtual Ground (AMG) - A New Scaling Concept for Very High-Density EPROM's," IEEE Electron Device Letters, pgs. 450-452, Vol. 12, No. 8, August 1991, IEEE	
	A125	BOAZ EITAN et al.: "Multilevel Flash cells and their Trade-offs," IEEE Electron Device Letters, pgs. 169-172, 1996, IEEE	
	A126	DR. HEINRICH ENDERT: "Excimer Lasers as Tools for Material Processing in Manufacturing," Technical Digest: International Electron Devices Meeting, 1985, pgs. 28-29, Washington, DC, December 1-4, 1985, Göttingen, Germany	

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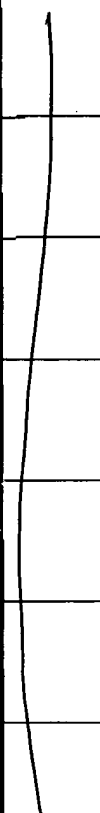

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		First Named Inventor	Thomas H. Lee et al.
		Group Art Unit	2818
		Examiner Name	Unassigned
Sheet	4	of	7
		Attorney Docket Number	035905/0104

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
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	A127	DOV FROHMAN-BENTCHKOWSKY: "A Fully Decoded 2048-Bit Electrically Programmable FAMOS Read-Only Memory," IEEE Journal of Solid-State Circuits, pgs. 301-306, Vol. 16, No. 5, October 1971	
	A128	G.K. GIUST et al.: "Laser-Processed Thin-Film Transistors Fabricated from Sputtered Amorphous-Silicon Films," IEEE Transactions on Electron Devices, pgs. 207-213, Vol. 47, No. 1, January 2000, IEEE	
	A129	G.K. GIUST et al.: "High-Performance Thin-Film Transistors Fabricated Using Excimer Laser Processing and Grain Engineering," IEEE Transactions on Electron Devices, pgs. 925-932, Vol. 45, No. 4, April 1998, IEEE	
	A130	G.K. GIUST et al.: "High-Performance Laser-Processed Polysilicon Thin-Film Transistors," IEEE Electron Device Letters, pgs. 77-79, Vol. 20, No. 2, February 1999, IEEE	
	A131	FUMIHIKO HAYASHI et al.: "A Self-Aligned Split-Gate Flash EEPROM Cell with 3-D Pillar Structure," 1999 Symposium on VLSI Technology Digest of Technical Papers, pgs. 87-88, Stanford University, Stanford, CA 94305, USA	
	A132	STEPHEN C.H. HO et al.: "Thermal Stability of Nickel Silicides in Different Silicon Substrates," Department of Electrical and Electronic Engineering, pgs. 105-108, 1998, IEEE	
	A133	J. ESQUIVEL et al.: "High Density Contactless, Self Aligned EPROM Cell Array Technology," Texas Instruments (Dallas), IEDM 86, pgs. 592-595, 1986, IEEE	
	A134	R. KAZEROUNIAN et al.: Alternate Metal Virtual Ground EPROM Array Implemented in a 0.8µm Process for Very High Density Applications," IEDM 91, pgs. 311-314, 1991, IEEE	
	A135	CHANG-DONG KIM et al.: "Short-Channel Amorphous-Silicon Thin-Film Transistors," IEEE Transactions on Electron Devices, pgs. 2172-2176, Vol. 43, No. 12, December 1996, IEEE	

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	A136	JOHAN H. KLOOTWIJK et al.: "Deposited Inter-Polysilicon Dielectrics for Nonvolatile Memories," IEEE Transactions on Electron Devices, pgs. 1435-1445, Vol. 46, No. 7, July 1999, IEEE	
	A137	WEBPAGE - JA-HUM KU et al.: "High Performance pMOSFETs With Ni(Si/sub x/Ge/sub 1-x Si/Sub 0.8/Ge/sub 0.2/ gate, IEEE Xplore Citation," VLSI Technology, 200. Digest of Technical Paper Symposium on page(s): 114-115 June 13-15 2000	
	A138	NAE-IN LEE et al.: "High-Performance EEPROM's Using N- and P-Channel Polysilicon Thin-Film Transistors with Electron Cyclotron Resonance N2O-Plasma Oxide," pgs. 15-17, IEEE Electron Device Letters, Vol. 20, No. 1, January 1999, IEEE	
	A139	JIN-WOO LEE et al.: "Improved Stability of Polysilicon Thin-Film Transistors under Self-Heating and High Endurance EEPROM Cells for Systems-On-Panel," IEEE Electron Device Letters, 1998, pgs. 265-268, IEEE	
	A140	SEOK-WOON LEE et al.: "Pd induced lateral crystallization of Amorphous Si Thin Films," Appl. Phys. Lett. 66 (13), pgs. 1671-1673, 27 March 1995, American Institute of Physics	
	A141	K. MIYASHITA et al.: "Optimized Halo Structure for 80 nm Physical Gate CMOS Technology with Indium and Antimony Highly Angled Ion Implantation," IEDM 99-645, pgs. 27.2.1-27.2.4, 1999, IEEE	
	A142	N.D. YOUNG et al.: "The Fabrication and Characterization of EEPROM Arrays on Glass Using a Low-Temperature Poly-Si TFT Process," IEEE Transactions on Electron Devices, pgs. 1930-1936, Vol. 43, No. 11, November 1996, IEEE	
	A143	JUNG-HOON OH et al.: "A High-Endurance Low-Temperature Polysilicon Thin-Film Transistor EEPROM Cell," pgs. 304-306, IEEE Electron Device Letters, Vol. 21, No. 6, June 2000, IEEE	
	A144	WEBPAGE - M.C. POON, et al.: "Thermal Stability of Cobalt and Nickel Silicides in Amorpho Crystalline Silicon," pg. 1, IEEE Xplore, Electron Devices Meeting, 1997, Proceedings, 19 Hong Kong, 2000, IEEE	

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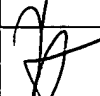
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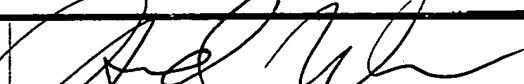
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		Examiner Name	Unassigned
		Attorney Docket Number	035905/0104
Sheet	6	of	7

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	A145	NORIAKI SATO et al.: "A New Programmable Cell Utilizing Insulator Breakdown," IEDM 85, pgs. 639-642, 1985, IEEE	
	A146	TAKEO SHIBA et al.: "In Situ Phosphorus-Doped Polysilicon Emitter Technology for Very High-Speed, Small Emitter Bipolar Transistors," IEEE Transactions on Electron Devices, pgs. 889-897, Vol. 43, No. 6, June 1996, IEEE	
	A147	SEUNGHEON SONG et al.: "High Performance Transistors with State-of-the-Art CMOS Technologies," IEDM 99, pgs. 427-430, 1999, IEEE	
	A148	YOSHIHIRO TAKAO et al.: "Low-Power and High-Stability SRAM Technology Using a Laser-Recrystallized p-Channel SOI MOSFET," IEEE Transactions on Electron Devices, pgs. 2147-2152, Vol. 39, No. 9, September 1992, IEEE	
	A149	KENJI TANIGUCHI et al.: "Process Modeling and Simulation: Boundary Conditions for Point Defect-Based Impurity Diffusion Model," IEEE Transactions on Computer-Aided Design, pgs. 1177-1183, Vol. 9, No. 11, November 1990, IEEE	
	A150	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, pgs. 391-393, Vol. 21, No. 9, September 2000, IEEE	
	A151	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, Vol. 21, No. 9, pgs. 439-441, September 2000, IEEE	
	A152	HONGMEI WANG et al.: "Super Thin-Film Transistor with SOI CMOS Performance Formed by a Novel Grain Enhancement Method," IEEE Transactions on Electron Devices, pgs. 1580-1586, Vol. 47, No. 8, August 2000, IEEE	
	A153	MARVIN H. WHITE et al.: "On the Go With Sonos," Circuit & Devices, pgs. 22-31, July 2000, IEEE	

Examiner Signature		Date Considered	10/3/03
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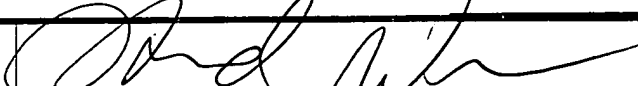
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	09/927,648
		Filing Date	08/13/2001
Date Submitted: <u>November 27, 2001</u> (use as many sheets as necessary)		First Named Inventor	Thomas H. Lee et al.
		Group Art Unit	2818
Sheet 7 of 7		Examiner Name	Unassigned
		Attorney Docket Number	035905/0104

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
	A154	B.J. WOO et al.: "A Novel Memory Cell Using Flash Array Contactless Eprom (Face) Technology," IEDM, pgs. 90-93, 1990, IEEE	
	A155	QI XIANG et al.: "Deep sub-100 nm CMOS with Ultra Low Gate Sheet Resistance NiSi," VLSI Technology, 2000. Digest of Technical Paper Symposium on... pgs. 76-77, IEEE Xplore, June 13-15, 2000	
	A156	QI XIANG et al.: "Deep Sub-100nm CMOS with Ultra Low Gate Sheet Resistance by NiSi," IEEE, pgs. 76-77, 2000, Symposium on VLSI Technology Digest of Technical Papers	
	A157	QIUXIA XU et al.: "New Ti-SALICIDE Process Using Sb and Ge Preamorphization for Sub-0.2 µm CMOS Technology," IEEE Transactions on Electron Devices, pgs. 2002-2009, Vol. 45, No. 9, September 1998, IEEE	
	A158	KUNIYOSHI YOSHIKAWA et al.: "An Asymmetrical Lightly Doped Source Cell for Virtual Ground High-Density EPROM's," IEEE Transactions on Electron Devices, pgs. 1046-1051, Vol. 37, No. 4, April 1990, IEEE	
	A159	JOHN R. LINDSEY et al.: "Polysilicon Thin Film Transistor and EEPROM Characteristics for Three Dimensional Memory," 198 th Meeting of The Electrochemical Society, Meeting Abstracts, Volume 2000-2, Phoenix, October 22-27, 2000	
	A160	VIVEK SUBRAMANIAN: "Control of Nucleation and Grain Growth in Solid-Phase Crystallized Silicon for High-Performance Thin Film Transistors," A Dissertation submitted to the Department of Electrical Engineering and the Committee of Graduate Studies of Stanford University, 1998	
	A161	BRIAN DIPERT: "Exotic Memories, Diverse Approaches," EDN Asia, September 2000	
	A162	DIETMAR GOGL et al.: "A 1-Kbit EEPROM in SIMOX Technology for High-Temperature Applications up to 250° C," IEEE Journal of Solid-State Circuits, October 2000, Vol. 35, No. 10, IEEE	

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Date Submitted: June 11, 2002

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of

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Complete if Known

Application Number	09/927,648
Filing Date	08/13/2001
First Named Inventor	Thomas H. LEE et al.
Group Art Unit	2818
Examiner Name	Unassigned
Attorney Docket Number	035905-0104

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document ²		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ³ (if known)			
	B1	4,500,905		Shibata		
	B2	6,185,122		Johnson et al.		
	B3	3,414,892		McCormack et al.	12/13/1968	
	B4	3,432,827		Sarno	3/11/1969	
	B5	4,535,424		Reid		
	B6	4,630,096		Drye		
	B7	4,672,577		Hirose		
	B8	4,710,798		Marcantonio		
	B9	4,811,082		Jacobs		
	B10	5,001,539		Inoue et al.		
	B11	5,089,862		Warner, Jr. et al.		
	B12	5,160,987		Pricer et al.		
	B13	5,191,405		Tomita et al.		
	B14	5,202,754		Bertin et al.		
	B15	5,266,912		Kledzik		
	B16	5,283,453		Stokes et al.		
	B17	5,398,200		Mazure et al.		
	B18	5,422,435		Taklar et al.		
	B19	5,426,566		Beilstein, Jr.		
	B20	5,434,745		Shokrgozar et al.		
	B21	5,453,952		Okudaira		
	B22	5,455,455		Kurtz et al.		
	B23	5,466,997		Imai et al.		
	B24	5,471,090		Deutsch		
	B25	5,481,133		Hsu		
	B26	5,495,398		Taklar et al.		
	B27	5,502,289		Taklar et al.		
	B28	5,523,622		Harada et al.		
	B29	5,523,628		Williams et al.		
	B30	5,552,963		Burns		
	B31	5,561,622		Bertin et al.		
	B32	5,581,498		Ludwig et al.		
	B33	5,585,675		Knopf		
	B34	5,612,570		Eide et al.		
	B35	5,654,220		Leedy		
	B36	5,693,552		Hsu		
	B37	5,696,031		Wark		
	B38	5,703,747		Voldman et al.		
	B39	5,780,925		Cipolla et al.		
	B40	5,781,031		Bertin et al.		
	B41	5,801,437		Burns		
	B42	5,915,157		Leedy		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	09/927,648
Date Submitted: June 11, 2002		Filing Date	08/13/2001
(use as many sheets as necessary)		First Named Inventor	Thomas H. LEE et al.
		Group Art Unit	2818
		Examiner Name	Unassigned
Sheet	2 of 7	Attorney Docket Number	035905-0104

U.S. PATENT DOCUMENTS				
	U.S. Patent Document			
B43	5,969,360		Syyedy	
B44	5,976,953		Zavracky et al.	
B45	5,985,693		Leedy	
B46	6,057,598		Payne et al.	
B47	6,072,234		Camien et al.	
B48	6,087,722		Lee et al.	
B49	6,133,640		Leedy	
B50	6,351,028		Akram	
B51	6,281,042	B1	Ahn et al.	
B52	6,291,858	B1	Ma et al.	
B53	6,307,257	B1	Huang et al.	
B54	6,314,013	B1	Ahn et al.	
B55	6,322,903	B1	Siniaguine et al.	
B56	6,337,521	B1	Masuda	
B57	6,353,265	B1	Michii	
B58	6,355,501	B1	Fung et al.	
B59	6,197,641	B1	Hergenrother et al.	

FOREIGN PATENT DOCUMENTS								
Examiner Initials	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
[Handwritten marks]	B60	EPC	0 073 486	A2	Toyama et al.	8-26-1982		
	B61	JP	61-222216		Yohehara	10-2-1986		
	B62	WO	94/26083		Carson et al.	11-10-1994		
	B63	EPO	0 516 866	A1	Bayer et al.	12-9-1992		
	B64	EPO	0 644 548	A2	Bertin	9-2-1994		
	B65	EPO	0 800 137	A1	Genduso et al.	3-14-1997		
	B66	EPO	0 606 653	A1	Harward et al.	7-20-1994		
	B67	EPO	0 395 886	A2	Oota et al.	11-7-1990		
	B68	JP	63-52463		Hitachi	3-5-1998		
	B69	JP	6-22352		Toshiba			
	B70	EPO	0 387 834	A2	Wada	9-14-1990		

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		Filing Date	08/13/2001
		First Name and Inventor	Thomas H. LEE et al.
		Group Art Unit	2818
		Examiner Name	Unassigned
Sheet 3 of 7	Attorney Docket Number	035905-0104	

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[Signature]	B71	ABOU-SAMRA S.J.: "3D CMOS SOI for High Performance Computing", Low Power Electronics and Design Proceedings, 1998.	
	B72	YAMAZAKI K.: "4-Layer 3-D IC Technologies for Parallel Signal Processing", International Electron Devices Meeting Technical Digest, December 9-12, 1990, pgs 25.5.1 - 25.5.4.	
	B73	SCHLAEPPPI H.P.: "nd Core Memories using Multiple Coincidence", IRE Transactions on Electronic Computers, June 1960, pgs 192 - 196.	
	B74	SCHLAEPPPI H.P.: "Session V: Information Storage Techniques", International Solid-State Circuits Conference, February 11, 1960, pgs. 54-55.	
	B75	DE GRAAF C. et al.: "A Novel High-Density, Low-Cost Diode Programmable Read Only Memory," IEDM, beginning at page 189	
	B76	PETER K. NAJI et al.: "A 256kb 3.0V 1T1MTJ Nonvolatile Magnetoresistive RAM," 2001 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC 2001/Session 7/Technology Directions: Advanced Technologies/7.6, February 6, 2001, pp. 122-123 (including enlargement of figures, totaling 9 pages), and associated Visual Supplement, pp. 94-95, 4040-405 (enlargements of slides submitted, totaling 25 pages)	
	B77	KIM C. HARDEE et al.: "A Fault-Tolerant 30 ns/375 mW 16K x 1 NMOS Static RAM," IEEE Journal of Solid-State Circuits, October 1981, Vol. SC-16, No. 5, pages 435-443	
	B78	TOSHIO WADA et al.: "A 15-ns 1024-Bit Fully Static MOS RAM," IEEE Journal of Solid-State Circuits, October 1978, Vol. SC-13, No. 5, pages 635-639	
	B79	CAMPERI-GINESTET C.: "Vertical Electrical Interconnection of Compound Semiconductor Thin-Film Devices to Underlying Silicon Circuitry", IEEE Photonics Technology Letters, Vol. 4, No. 9, September 1992, pgs. 1003-1006.	
	B80	AKASAKA YOICHI: "Three-dimensional Integrated Circuit: Technology and Application Prospect", Microelectronics Journal, Vol. 20, No.s 1-2, 1989, pgs. 105 - 112.	
[Signature]	B81	SAKAMOTO KOJI: "Architecture des Circuits a Trois Dimension (Architecture of Three Dimensional Devices)", Bulletin of the Electrotechnical Laboratory, ISSN 0366-9092, Vol. 51, No. 1, 1987, pgs 16 - 29.	
	B82	AKASAKA YOICHI: "Three-dimensional IC Trends", "Proceedings of the IEEE, Vol. 74, No. 12, 1986, Pgs. 1703 - 1714.	

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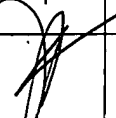
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: June 11, 2002 <i>(use as many sheets as necessary)</i>		Application Number	09/927,648
		Filing Date	08/13/2001
		First Named Inventor	Thomas H. LEE et al.
		Group Art Unit	2818
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Sheet 4 of 7	Attorney Docket Number	035905-0104	

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	B83	CARTER WILLIAM H.: "National Science Foundation (NSF) Forum on Optical Science and Engineering", Proceedings SPIE - The International Society for Optical Engineering, Vol. 2524, July 11 - 12 1995, (Article by N. Joverst titled "Manufacturable Multi-Material Integration Compound Semi-conductor Devices Bonded to Silicon Circuitry")	
	B84	HAYASHI Y.: "A New Three Dimensional IC Fabrication Technology, Stacking Thin Film Dual-CMOS Layers", IEDM, 1991, pgs. 25.6.1 - 25.6.4.	
	B85	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEEE, 1996, pgs. 121-124.	
	B86	STERN JON M.: "Design and Evaluation of an Epoxy Three-dimensional Multichip Module, IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, February 1996, pgs 188-194.	
	B87	BERTIN CLAUDE L.: "Evaluation of a Three-dimensional Memory Cube System", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 16, No. 8, December 1993, pgs. 1006 - 1011.	
	B88	WATANABE HIDEHIRO: "Stacked Capacitor Cells for High-density Dynamic RAMs", IEDM, 1988, pgs. 600 - 603.	
	B89	WEB PAGE: "Stacked Memory Modules", IBM Technical Disclosure Bulletin, Vol. 38, No. 5, 1995.	
	B90	THAKUR SHASHIDHAR: "An Optimal Layer Assignment Algorithm for Minimizing Crosstalk for Three VHV Channel Routing", IEDM, 1995, pgs. 207 - 210.	
	B91	TERRIL ROB: "3D Packaging Technology Overview and Mass Memory Applications", IEDM, 1996, pgs. 347 - 355.	
	B92	INOUE Y.: "A Three-Dimensional Static RAM", IEEE Electron Device Letters, Vol. 7, No. 5, May 1986, pgs. 327 - 329.	
	B93	REBER M.: "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic", IEDM, 1996, pgs. 121 - 124.	
	B94	KUROKAWA TAKAKAZU: "3-D VLSI Technology in Japan and an Example: A Syndrome Decoder for Double Error Correction", FGCS - Future, Generation, Computer, Systems", Vol. 4, No. 2, 1988, pgs. 145-155, Amsterdam, The Netherlands.	

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		Filing Date	08/13/2001
		First Named Inventor	Thomas H. LEE et al.
		Group Art Unit	2818
		Examiner Name	Unassigned
		Attorney Docket Number	035905-0104
Sheet	5	of	7

B95	MAKINIAK DAVID: "Vertical Integration of Silicon Allows Packaging of Extremely Dense System Memory In Tiny Volumes: Memory-chip Stacks Send Density Skyward", Electronic Design, No. 17, August 22, 1994, pgs. 69-75, Cleveland Ohio.
B96	YAMAZAKI K.: "Fabrication Technologies for Dual 4-KBIT Stacked SRAM", IEDM 16.8., 1986, pgs. 435-438.
B97	PEIN HOWARD: "Performance of the 3-D PENCIL Flash EPROM Cell an Memory Array", IEEE Transactions on Electron Devices, Vol. 42, No. 11, November 1995, pgs. 1982-1991.
B98	Abstract LOMATCH S.: "Multilayered Josephson Junction Logic and Memory Devices", Proceedings of the SPIE-The International Society for Optical Engineering Vol. 2157, pgs. 332-343.
B99	Abstract LU N.C.C.: "Advanced Cell Structures for Dynamic RAMs", IEEE Circuits and Devices Magazine, Vol. 5, No. 1, January 1989, pgs. 27-36.
B100	Abstract SAKAMATO K.: "Architecture of Three Dimensional Devices", Journal: Bulletin of the Electrotechnical Laboratory, Vol. 51, No. 1, 1987, pgs. 16-29.
B101	Abstract "Wide Application of Low-Cost Associative Processing Associative Processing Seen", Electronic Engineering Times, August 26, 1996, pg. 43.
B102	Abstract "Interconnects & Packaging", Electronic Engineering Times, November 27, 1995, pg. 43.
B103	Abstract "Closing in on Gigabit DRAMs", Electronic Engineering Times, November 27, 1995, pg. 35.
B104	Abstract "Module Pact Pairs Cubic Memory with VisionTek", Semiconductor Industry & Business Survey, Vol. 17, No. 15, October 23, 1995.
B105	Abstract "Layers of BST Materials Push Toward 1Gbit DRAM", Electronics Times, October 19, 1995.
B106	Abstract "Technologies Will Pursue Higher DRAM Densities", Electronic News (1991), December 4, 1994, pg. 12.

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		Filing Date	08/13/2001
		First Named Inventor	Thomas H. LEE et al.
		Group Art Unit	2818
		Examiner Name	Unassigned
		Attorney Docket Number	035905-0104
Sheet	6	of	7

B107	Abstract "Looking Diverse Storage", Electronic Engineering Times, October 31, 1994, pg. 44.
B108	Abstract "Special Report: Memory Market Startups Cubic Memory: 3D Space Savers", Semiconductor Industry & Business Survey, Vol. 16, No. 13, September 12, 1994.
B109	Abstract "Technique Boosts 3D Memory Density", Electronic Engineering Times, August 29, 1994, pg. 16.
B110	Abstract "Memory Packs Poised 3D Use", Electronic Engineering Times, December 7, 1992, pg. 82.
B111	Abstract "MCMs Hit the Road", Electronic Engineering Times, June 15, 1992, pg. 45.
B112	Abstract "IEDM Ponders the 'Gigachip' Era", Electronic Engineering Times, January 20, 1992, pg. 33.
B113	Abstract "Tech Watch: 1-Gbit DRAM in Sight", Electronic World News, December 16, 1991, pg. 20.
B114	Abstract "MCMs Meld into Systems", Electronic Engineering Times, July 22, 1991, pg. 35.
B115	Abstract "Systems EEs See Future in 3D", Electronic Engineering Times, September 24, 1990, pg. 37.
B116	Patent Application, NISHIURA, US 2001/00054759 A1.
B117	Patent Application, FURUSAWA, US 2002/0024146 A1.
B118	Patent Application, FUJIMOTO et al, US 2002/0027275 A1.

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Sheet 7 of 7	Attorney Docket Number	035905-0104	

B119	Patent Application, AKRAM, US 2002/0030262 A1.
B120	Patent Application, AKRAM, US 2002/0030263 A1.
B121	Patent Application, LEEDY, US 2001/0033030 A1.
B122	Chan et al. "Three Dimensional CMOS integrated Circuits on Large Grain Polysilicon Films" IEEE, Hong Kong University of Science and Technology 2000 IEEE

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